PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER USING AUTOMATIC LOOP CONTROL AND METHOD OF OPERATION

ABSTRACT OF THE DISCLOSURE

A (PLL) frequency synthesizer comprising: 1) a VCO that generates a first clock having frequency, Fout, determined by a loop filter control voltage; 2) a first divider for dividing Fout by N to produce a second clock of frequency, Fout/N; 3) a second divider for dividing a reference frequency, Fin, by M to produce a third clock of frequency, Fin/M; 4) a phase-frequency detector for comparing the second and third clocks, generating an UP signal if the second clock is slower than the third clock, and generating a DOWN signal if the second clock is faster than the third clock; 5) a charge pump that receives the UP and DOWN signals and increases or decreases the control voltage on the loop filter by injecting or draining a charge pump current, Ic; and 6) a loop response control circuit for adjusting Ic as a function of N and M.